REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated December 17, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 13-18 are under consideration in this application. Claims 1-8 are being cancelled without prejudice or disclaimer. New claims 13-18 are being added to recite other embodiments described in the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejection

Claims 1-6 were rejected under 35 U.S.C. 102(e) on the grounds of being anticipated by U.S. Pat. No. 6,269,036 to Shubat (hereinafter "Shubat"), and claims 1, 6 and 7 were further rejected under 35 U.S.C. 102(b) on the grounds of being anticipated by U.S. Pat. No. 5,805,514 to Iwakiri (hereinafter "Iwakiri"). Further, claim 8 was rejected under 35 U.S.C. 103(a) on the grounds of being unpatentable over Iwakiri in view of U.S. Pat. No. 6,058,056 to Beffa et al. (hereinafter "Beffa"). The prior art references of Kuromiya et al. (6,034,904), Kumakura (5,892,776), Ohtani et al. (6,297,997) and Tsukikawa (6,061,285) were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed, as more fully discussed below.

The semiconductor integrated circuit device of the invention (e.g., Figs. 6-7), as now recited in claim 13, comprises: a first terminal which receives a first clock signal CLK (e.g., 333 MHz) outside of said semiconductor integrated circuit device; a second terminal which receives an address signal RAS outside of said semiconductor integrated circuit device; a third terminal which receives a second clock signal DGCLK (e.g., 33 MHz) outside of said semiconductor integrated circuit device, said second clock signal has a frequency lower than a frequency of the first clock signal; a delay circuit Delay which delays said address signal RAS (also RAS1 -> RAS2); a control circuit (including the DFT circuit) which receives said first clock signal CLK, said second clock signal DGCLK, and said address signal RAS, and outputs a control signal (Test

Mode Flag) in accordance with whether said semiconductor integrated circuit is in a normal operation mode or a test mode **for testing at least one of a write time** tRWL **and a bit-line percharge time** tPR (p. 39, lines 18-20); and a memory circuit which receives said control signal, and includes a plurality of word lines, a plurality of bit lines, and a plurality of memory cells. In the normal operation mode, a selecting operation of one of said plurality of word lines is terminated by an output RAS2 of said delay circuit (Fig. 7; "*during the normal operation, the internal RAS formed by the aforementioned latch circuit (G1, G2) starts the memory selecting operation by activating the internal RAS* (L->H) *by the active level* (H->L) *fetched in synchronism with CLK, and terminates the memory selecting operation by deactivating the internal RAS by the inactive level* (L->H) *of the signal RAS2 formed by delaying by the delay circuit Delay the inactive level* (L->H) *of the RAS signal fetched in synchronism with CLK*" p. 36, last paragraph). In the test mode, another selecting operation of one of said plurality of word lines operation is terminated by the second clock signal DGCLK (Fig. 7; "As shown in the timing chart in Fig. 7, in the test mode, ... *to terminate the memory selecting operation [in the test mode] by deactivating the internal RAS by the active level* (H->L) *of the clock signal DGCLK ... instead of the aforementioned signal RAS2*" p. 38, line 24 – p. 39, line 6).

In other words, the delay circuit delays the address signal RAS1 into RAS2 with a delay time TD to terminate the word line selection operation in normal operation by RAS2 an din the test mode by the second clock signal DGCLK (Fig. 7; "*A signal RAS2 obtained by delaying this signal RAS1 by a delay circuit Delay ..., and is used as a reset signal for resetting the aforementioned latch circuit (G1, G2)* p. 36, lines 12-17; "*The aforementioned delay circuit Delay is provided for adding a delay time TD to the time duration when the RAS signal synchronized with the clock signal CLK changes from the active level to the inactive level in the memory operation period* (p. 37, lines 2-6).".

Accordingly, the invention resolves the problems caused by using a lower-speed clock in test mode, such as write failure due to faulty bit cells (in solid lines in Figs. 8A-B; p. 39, line 21-p.40, line 25) and bit-line precharge failure (in solid lines in Figs. 9A-B; p. 41, line 11 – p. 42, line 10)). The invention affects the time length of the memory selecting operation in the test mode as shown in dotted lines in Figs. 8A-B. "B*y using the test mode, the fall timing of the word line WL is changed over from an edge trigger of the normal clock (CLK) to an edge trigger of the clock (DGCLK) used exclusively for testing*" "*The fall time of the word line WL is* ***advanced[shortened]*** *by a time TW, so that the write time is set to the same as that during the*

above-described actual operation to permit the test. The faulty bits can be detected and can be remedied in the wafer state." See p. 40, line 26- p. 41, line 10. The invention further affects the time length of precharging operation in the test mode as shown in solid lines in Figs. 9A-B. "*By using the same test mode as that during the aforementioned write time tRWL, the word line WL is made to fall at the same timing as that in the actual high-speed operation by* ***delaying*** *the fall time of the word line WL by a time TP, so that the bit-line precharge time is set to the same as that during the high-speed operation to permit the test. Thus such faulty bits can be detected and can be remedied in the wafer state* (p. 42, lines 11- 24)." In short, the invention delays the address signal RAS1 to provide RAS2, which works in conjunction with RAS1 and DGCLK to provide an internal RAS as shown in the bottom of Fig. 7 with desirable normal mode and test mode timing.

Applicant respectfully submits that none of the cited prior art references discloses, teaches or suggests such "a delay circuit for delaying the address signal RAS1 to provide RAS2 to terminate a selecting operation of one of said plurality of word lines in the normal operation mode, while the second clock signal DGCLK is used to terminate another selecting operation of one of said plurality of word lines operation in the test mode" so as to provide an internal RAS as shown in the bottom of Fig. 7 with desirable normal mode and test mode timing for testing at least one of a write time and a bit-line percharge time according to the invention.

In contrast, Shubat activates both word lines active simultaneously to test whether both word lines will be enabled at the same time during normal mode to allow worst case testing (col. 2, lines 6-8) so as to find out defects due to clock skew or accessing both word lines simultaneously (col. 2, lines 19-22). Shubat merely tests "*multiple port memory devices that effectively test for the* ***most stressful conditions*** *and* ***accounts for clock skew*** (col. 3, lines 7-8)", rather than "at least one of a write time tRWL and a bit-line percharge time tPR" which motivated the design of "providing a delay circuit for delaying the address signal RAS1 to provide RAS2 to terminate a selecting operation of one of said plurality of word lines in the normal operation mode, while using the second clock signal DGCLK to terminate another selecting operation of one of said plurality of word lines operation in the test mode" of the invention.

Furthermore, Shubat teaches away from the invention by ***countering*** (rather than "***increasing/promoting***") delay in the generation of the CCLK and EQ signals so as to minimize the operational delay introduced by addition of the test circuitry. "*Essentially, the transistor 634*

and its coupling to the TEST signal blocks transitions in the clock signal by not letting the clock cycle stop. This implementation is particularly advantageous because it introduces much less delay in the generation of the CCLK and EQ signals. Especially for high-speed designs, this is critical and minimizes the operational delay introduced by addition of the test circuitry (col. 8, lines 29-35). " It is well established that a rejection based on cited references having principles that teach away from the invention is improper.

Iwakiri performs a test "by inputting a test mode signal to the semiconductor memory device to initiate the specified test, delaying generation of the reset signal for a period of time exceeding the predetermined period of time, carrying out the specified test while the test mode signal is being input, and terminating the specified test by stopping input of the test mode signal (Abstract)." As Iwakiri' second embodiment shown in Figs. 3-4, the delay circuit 41 delays the reset signal S4 generated by the ROW-system control circuit 15 into a reset signal Sd (Fig. 4) which reaches the clock generating circuit 13 by a delay Td (col. 7, lines 49-51). In the test state (col. 7, line 42), Iwakiri delays the stopping time for generating CK thereby extending the operating time for a fundamental operation such as activating a word line, rendering a sense amplifier active, etc (col. 7, lines 51-57). In Iwakiri's test state, a selecting operation of one of said plurality of word lines operation is terminated by an output Sd of the delay circuit 41, rather than any second clock signal used exclusively for testing DGCLK according to the invention. Applicants further contend that the alleged second clock signal used exclusively for testing CKt is not available in Iwakiri's second embodiment and there is no teaching to combine the first and second embodiments.

Furthermore, Iwakiri merely tests "for a short circuit between a bit line and a cell plate (Abstract)," rather than "at least one of a write time tRWL and a bit-line percharge time tPR" which motivated the design of "providing a delay circuit for delaying the address signal RAS1 to provide RAS2 to terminate a selecting operation of one of said plurality of word lines in the normal operation mode, while using the second clock signal DGCLK to terminate another selecting operation of one of said plurality of word lines operation in the test mode" of the invention.

Iwakiri's delay Td is "*sufficient to extend the time required for the reset signal S4 to reach the clock generating circuit 13 so that the operating time during which a fundamental operation of the semiconductor memory device can be carried out for the purpose of conducting a test is longer than the operating time for a fundamental operation to be carried out in the*

ordinary use of the semiconductor memory device. Accordingly, if an abnormal state exists in the memory device, the operating time of the fundamental operation is ***extended/lengthened*** (col. 6, lines 53-62)". On the other hand, the invention ***advances/shortens*** the fall time of the word line WL by a time TW (Fig. 8B; p. 41, line 7) in testing a write time while delays/lengthens the fall time of the word line WL by a time TP (Fig. 9B; p. 42, line 20) in testing a bit-line precharge time.

Beffa simply fails to compensate for the above-mentioned deficiencies.

Applicants contend that the cited prior art references and their combinations fail to teach or disclose each and every feature of the present invention as disclosed in independent claim 13. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

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